

REMARKS

Claims 1, 2, 5-14, and 19-21 are now pending in the application. Claims 3-4 and 15-18 were cancelled herein. The Examiner is respectfully requested to reconsider and withdraw the rejection(s) in view of the amendments and remarks contained herein.

Applicant respectfully disputes the Examiner's position that the circuit defined by inverters 2₁ and 2₂ and the variable resistance produced by a transistor 4 with feedback 5 or 6 (as shown in FIGs. 1 and 6 of Matsuyama) function as a zero order transimpedance amplifier (TIA). In the interests of expediting prosecution, however, Applicant has incorporated dependent Claims 3 and 4 into independent Claim 1 and dependent Claims 15-18 into independent Claim 14. These amendments define a different structure than the Matsuyama circuit arrangement. Applicant reserves the right to reassert Claims 1 and 14 as originally filed in one or more continuing applications.

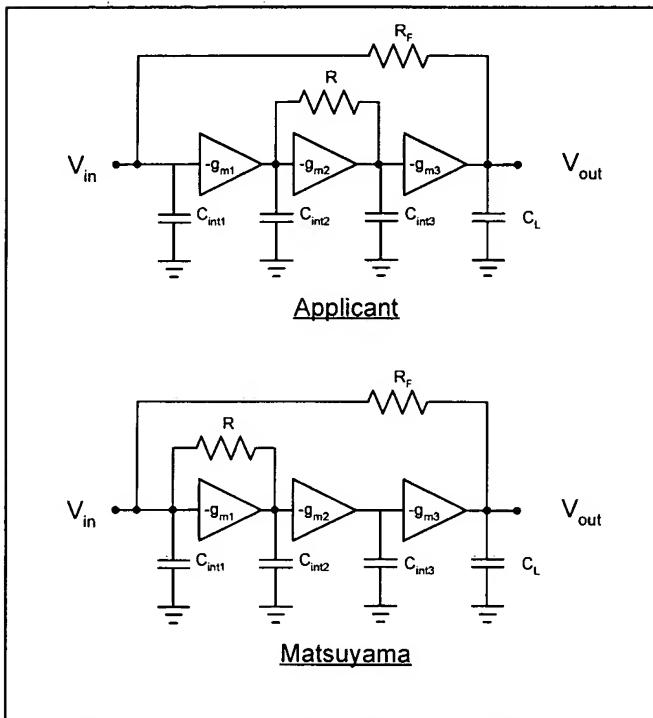
REJECTION UNDER 35 U.S.C. § 103

Claims 1, 9, 14-16, 20 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuyama (JP406061752A) in view of Holt "Electronic Circuits Digital and Analog". This rejection is respectfully traversed.

Regarding Claim 1, none of the references show, teach or suggest a zero order TIA that includes second and third opamps connected in series with a feedback resistance connected between the input and output of the third opamp and that is nested within a first opamp and feedback resistance as claimed.

In a phone conference with the Examiner on December 23, 2003, Applicant proposed amending independent Claims 1 and 14 to further define the claimed zero

order TIA. In other words, the Matsuyama circuit arrangement includes a feedback resistance R that is connected to the input and output of the opamp that is labeled $-g_{m1}$



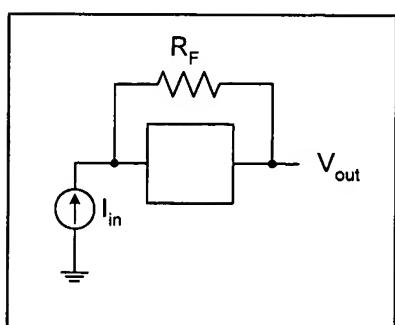
below (corresponding to inverter 2_1 in FIG. 1 of Matsuyama). In contrast, the feedback resistance R in Applicant's zero order TIA is connected to the input and output of the opamp that is labeled $-g_{m2}$ below. The currently claimed structure is different than the circuit arrangement that is disclosed by Matsuyama.

The following discussion sets

forth the gain and bandwidth for the Matsuyama circuit arrangement and the TIA circuit disclosed by Applicant. This analysis assumes that the same values are used for all of the components. To correctly identify the bandwidth, internal capacitances C_{int} for each of the opamps must be considered. In addition, a load capacitor C_L is also shown. Circuit schematics for both of these circuits are provided above. To simplify the discussion, the Matsuyama circuit arrangement will employ a fixed resistance rather than a variable resistance as disclosed. However, Applicant's arguments do not change

when a variable resistance is employed.

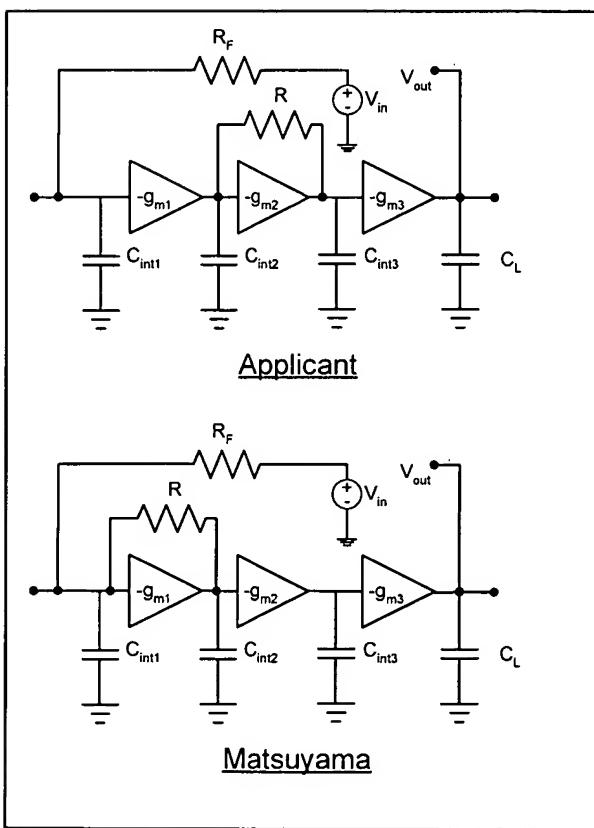
The most relevant characteristics of a TIA circuit are gain and bandwidth. As can be seen at left, both Applicant's TIA and the Matsuyama circuit arrangement



can be represented by a higher-level schematic. The differences between the circuits lie in the block between the opposite ends of the feedback resistance R_F . The gain for both

circuits is defined as $Gain = \frac{V_{out}}{I_{in}} = R_F$. The bandwidth (BW) of the two circuits, however,

is different. In the Matsuyama circuit arrangement, when R_F is increased to increase the gain, the bandwidth of the circuit decreases. In contrast, when R_F is increased in Applicant's TIA circuit, the bandwidth is not impacted.



In order to derive the bandwidth, the open loop response technique is used. The technique of looking at the open loop response provides information relating to the bandwidth and maximum achievable bandwidth of a circuit. The DC gain of the open loop response is determined by opening the feedback loop and attaching a voltage source to one end of the feedback resistor R_F as shown at left. The output voltage is sensed at the output node as shown at left. To derive the bandwidth, the

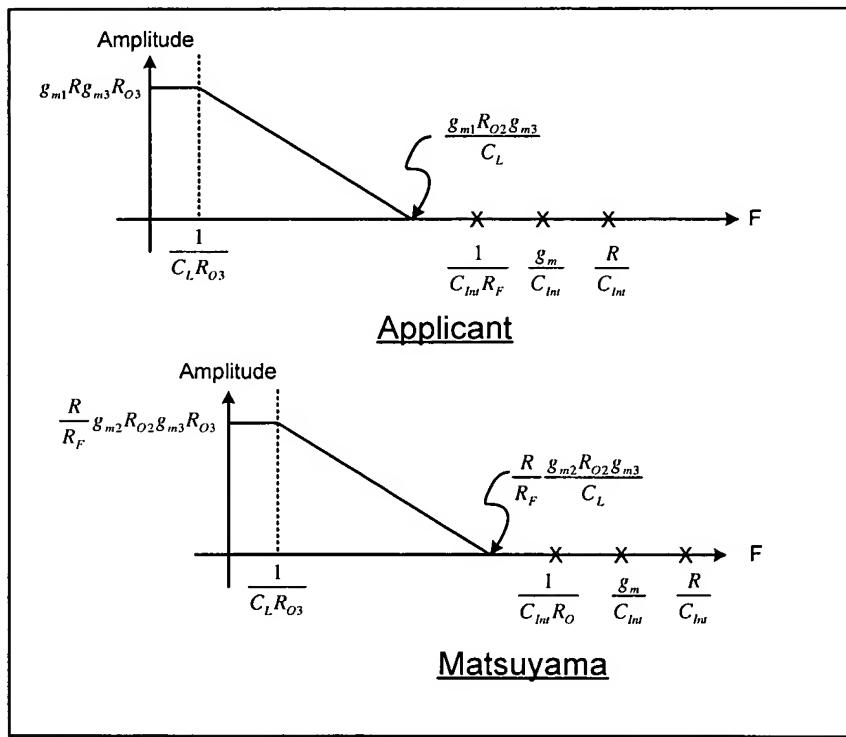
DC gain of the open loop response and the first dominant pole P_1 are found. Assuming stable operation, there is only one pole P_1 located below the crossover frequency. The crossover frequency is the product of the DC gain of the open loop response and the first dominant pole P_1 . The crossover frequency defines the bandwidth of the main

closed loop amplifier. The maximum available bandwidth is related to the second non-dominant pole P_2 .

The DC gain of the open loop response of the Matsuyama circuit arrangement is

$\frac{R}{R_F} g_{m2} R_{O2} g_{m3} R_{O3}$. The Matsuyama circuit has a dominant pole at $\frac{1}{C_L R_{O3}}$. Multiplying the

DC gain of the open loop response with P_1 results in the crossover frequency of the



Matsuyama circuit arrangement of

$\frac{R}{R_F} \frac{g_{m2} R_{O2} g_{m3}}{C_L}$. As can be

seen, the crossover frequency is inversely proportional to R_F (or gain). In other words as the gain is increased, the bandwidth is decreased.

Further the Matsuyama

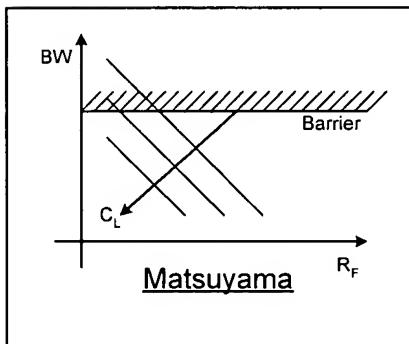
circuit arrangement has a non-dominant pole at $\frac{1}{R_0 C_{int}}$, which relates to a barrier

frequency or maximum achievable bandwidth.

In contrast, the DC gain of the open loop response of Applicant's TIA circuit is $g_{m1} R g_{m3} R_{O3}$, and Applicant's TIA has a dominant pole at $\frac{1}{C_L R_{O3}}$. The crossover frequency of Applicant's TIA circuit is $\frac{g_{m1} R_{O2} g_{m3}}{C_L}$. As is readily apparent, the crossover

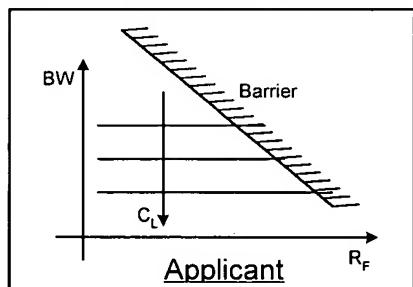
frequency is **not** dependent on R_F . Applicant's TIA circuit has a non-dominant pole at $\frac{1}{C_{int} R_F}$, which relates to the barrier frequency.

The closed loop gain of both the Matsuyama circuit arrangement and Applicant's TIA circuit are determined by the value of the feedback resistance R_F . The closed loop gain increases as a function of the feedback resistance R_F . The bandwidth of the



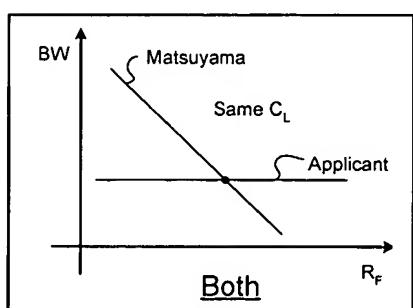
Matsuyama circuit arrangement, however, is inversely proportional to the feedback resistance R_F . In other words, as gain is increased by increasing R_F , the bandwidth decreases. This characteristic of the Matsuyama circuit arrangement forces a tradeoff between

the closed loop gain and bandwidth for different values of the load capacitance C_L as shown above. In contrast, the bandwidth of Applicant's TIA circuit is not dependent upon the feedback resistance R_F . In other words, as gain is increased by increasing R_F ,



there is no effect on bandwidth.

Assuming that both Applicant's TIA circuit and the Matsuyama circuit arrangement have the same load capacitance C_L , Applicant's circuit can achieve higher bandwidth than the Matsuyama circuit arrangement at higher gain values as shown at left.



As was demonstrated above, Applicant's TIA circuit arrangement has both a different structure and different operating characteristics than the Matsuyama

circuit arrangement. Therefore, independent Claim 1 is in allowable form. Claims 5-13

depend directly and/or indirectly on Claim 1 and are therefore also in allowable form for the same reasons.

Claim 14 was amended to further define the zero order TIA circuit in a manner that is similar to Claim 1 and is therefore also in allowable form. Claims 19-21 depend directly and/or indirectly on Claim 14 and are therefore in allowable form for the same reasons.

ALLOWABLE SUBJECT MATTER

Applicant would like to thank the Examiner for favorable consideration of Claims 7, 8 and 19, which were previously indicated as allowable if rewritten in independent form. Applicant reserves the right to rewrite Claims 7, 8 and 19 into independent form in their previously allowed status at a later date if needed.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: 1/22/04

By: Michael D. Wiggins
Michael D. Wiggins
Reg. No 34,754

MARVELL SEMICONDUCTOR, INC.
700 FIRST AVENUE, MAIL STOP 509
SUNNYVALE, CA 94089
408-222-2500